IN THE CLAIMS:

Sub D1

1. A method of assigning a buffer size in a video decoder, said method comprising the steps of:

establishing a first buffer size for a scalable buffer;

processing a video data stream utilizing said first buffer size;

selecting a second buffer size for said scalable buffer;

processing said video data stream utilizing said second buffer size;

creating memory utilization data characterizing memory performance during processing with said first buffer size and said second buffer size; and

assigning a buffer size for said scalable buffer in accordance with said memory utilization data.

2. The method of claim 1 wherein said establishing step and said selecting step each include the step of defining a buffer size as a multiple of an encoded image data block in the form of a macroblock.

3. The method of claim 1 wherein processing of said video data stream includes utilizing said scalable buffer with a variable length decoder.

4. The method of claim 1 wherein processing of said video data stream includes utilizing said scalable buffer with an inverse discrete cosine transfer function module.

5. The method of claim 1 wherein processing of said video data stream includes utilizing said scalable buffer with a motion compensator.

6. The method of claim 1 wherein said creating step includes the step of creating cache utilization data defining data cache miss rates.

7. The method of claim 1 wherein said creating step includes the step of creating cache utilization data defining instruction cache miss rates.

8. The method of claim 1 further comprising the step of modifying the size of video data stream processing instructions to correspond to said buffer size selected in said assigning step.

9. The method of claim 8 wherein said modifying step includes the step of loop unrolling data stream processing instructions to correspond to said buffer size selected in said assigning step.

10. A method of assigning a buffer size in a video decoder, said method comprising the steps of:

establishing a first buffer size for a scalable buffer;

processing said video data stream with said scalable buffer configured to said first buffer size;

selecting a second buffer size for said scalable buffer;

processing said video data stream with said scalable buffer configured to said second buffer size;

creating memory utilization data characterizing memory performance during processing with said scalable buffer at said first buffer size and said second buffer size; and

assigning a buffer size for said scalable buffer in accordance with said memory utilization data.

11. The method of claim 10 wherein said creating step includes the step of creating cache utilization data defining data cache miss rates.

12. The method of claim 10 wherein said creating step includes the step of creating cache utilization data defining instruction cache miss rates.

13. A computer readable memory to direct a computer to function in a specified manner, comprising:

a buffer management module to establish a first buffer size and a second buffer size for a scalable buffer;

a video decoding module to process a video stream utilizing said first buffer size and said second buffer size; and

an analysis module to create memory utilization data characterizing memory performance during processing with said first buffer size and said second buffer size, said analysis module including a buffer size adjuster to assign a buffer size for said scalable buffer in accordance with said memory utilization data.

14. The computer readable memory of claim 13 wherein said buffer management module establishes said first buffer size as a first multiple of an encoded image data block and said second buffer size as a second multiple of an encoded image data block.

15. The computer readable memory of claim 14 wherein said buffer management module establishes said first buffer size as a first multiple of a data macroblock associated with said video data stream and said second buffer size as a second multiple of a data macroblock associated with said video data stream.

16. The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a variable length decoder.

17. The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with an inverse discrete cosine transfer function module.

18. The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a motion compensator.

19. The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining data cache miss rates.

20. The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining instruction cache miss rates.

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